AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph beginning on page 10, line 17 as follows:

The circuit 126 may be implemented, in one example, as a skew control logic circuit. The circuit 126 may have a number of inputs 150a-150n that may receive the signals CLK1-CLKn and an input 152 that may receive a signal (e.g., SKEW_CONTROL). The circuit 126 may be configured to generate a number of signals (e.g., the signals CPUCLK, SDRAM, AGPCLK, PCICLK, APIC, etc.) in response to the signal SKEW_CONTROL and the signals CLK1-CLKn. The signal SKEW_CONTROL may control an amount of skew between, for example, the signals CPUCLK, SDRAM, AGPCLK, PCICLK, and APIC. For example, the circuit ~~120~~ 126 may be used to delay or pull-in the signal CPUCLK (or any other signal) by a preset value (e.g., within a range of 150 ps to 600 ps) relative to other signals or signal groups. In another example, the skew of one or more of the signals CPUCLK, SDRAM, AGPCLK, PCICLK, and APIC may be relative to one or more others of the signals CPUCLK, SDRAM, AGPCLK, PCICLK, and APIC. The skew may be controlled for any one or combination of the signals CPUCLK, SDRAM, AGPCLK, PCICLK, and APIC.

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